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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,653	01/18/2002	Constantin Bulucea	NS-5127 US	9448

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EXAMINER	
FARAHANI, DANA	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,653	BULUCEA, CONSTANTIN	
	Examiner	Art Unit	
	Dana Farahani	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60 and 69-94* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60 and 69-94* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 10-12, 29, 32, 33, 39, and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakai (US Patent 4,529,994), previously cited.

With regard to claims 1, 10-12, 29, 32, 33, 39, and 40, Sakai discloses in figure 3 a structure comprising a varactor comprising (a) a plate region 14 and a body region 11 of a semiconductor body, (b) a plate electrode 16 and a body electrode 18 respectively connected to the plate and body regions, (c) a gate dielectric 24 layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode 25 situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body region being of opposite conductivity types, and meeting each other to form a p-n junction (see column 2, lines 40-55), an inversion layer 19 occurring in the body region along the gate dielectric layer below the gate electrode, the inversion layer comprising multiple variably appearing inversion portions (at the middle and the sides of region 19, where there are different thickness); and an electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor.

With regard to claim 2, Sakai discloses the inversion portions (the middle portion of region 19 and the narrower portion at the left hand side of the middle portion), when present, meet the plate region.

With regard to claim 3, there is a first inversion portion (the left-hand-side portion) of the inversion layer and a second inversion portion (the narrow portion of the inversion portion 19), which is spaced apart from the plate region.

With regard to claims 4 and 5, the inversion portions 19 include a third inversion portion (at the right-hand-side portion of the middle portion of region 19), which is also spaced apart from the plate region.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 7-9, and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai as applied to claim 1 above, and further in view of US Patent Application Publication 2002/0036311 (US SN 09/961,248) issued to Hattori, previously cited.

With regard to claims 6, 7, 9, 34, and 37, Sakai discloses the claimed invention, as discussed above, except for multiple gate dielectric portions.

Hattori discloses in figure 2, multiple gate dielectric portions 10, with different thicknesses. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the gate dielectric portions of the Sakai's device with different thicknesses in order to have different capacitances (note that in claims 7 and 9, there is another thinner dielectric portion at the right of the middle, thicker portion of the gate dielectric region).

With regard to claims 8, 35 and 36, note that Hattori discloses in figure 2, the gate dielectric portions 10 comprises two dielectric portions, a first portion 3, and a second portion to the right of 3, which is thicker than the first portion, and the first portion would have extended, if incorporated in the Sakai's structure, to a location above the plate region, and the second region would have spaced laterally apart from the plate region of the Sakai reference.

5. Claims 13, 17, 18, 42, 44, 45, 53, 57, and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai as applied to claim 1 above, and further in view of the Japanese patent 04199682, previously cited.

Sakai discloses the claimed invention, as discussed above, except for multiple gate portions with different conductivity/dopant concentration parts.

The Japanese patent discloses in figure 2(b), a gate electrode portion with different conductivity type parts 4 and 5. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the gate structure in the Sakai's deice to have different portion with opposite conductivity types in order to have a larger current drive capacity (see the abstract).

6. Claims 14, 15, 16, 43, and 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai in view of the Japanese patent, as applied to claim 13 above, and further in view of Fratin et al, hereinafter Fratin (US Patent 5,977,591), previously cited.

Sakai in view of the Japanese patent discloses the limitations in the claims, as discussed above, but does not disclose the gate electrode has portions of the same conductivity type with different doping concentrations.

Fratin discloses in figure 1, and column 6, lines 23-33, a gate portion which has two potions of the same conductivity type, but different doping concentrations. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the gate of the structure of Sakai in view of the Japanese patent as such in order to adjust the capacitance of the device.

7. Claims 19 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai in view of the Japanese patent as applied to claim 17 above, and further in view of Iwamuro (US Patent 5,659,185), previously cited.

Sakai in view of the Japanese patent discloses the limitations in the claims, as discussed above, but does not disclose the gate electrode portions are shorted together.

Iwamuro discloses in figure 1, gate portions 12 are shorted together, as can be seen in the figure. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the two gate portions function as one gate portion, while maintaining the advantages of having isolated gate portions.

8. Claims 20, 21, 51, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai in view of the Japanese patent as applied to claim 13 above, and further in view of Pramanick et al., hereinafter Pramanick (US Patent 6,165,902), previously cited.

Sakai in view of the Japanese patent discloses the limitations in the claims, as discussed above, but does not disclose a polycrystalline gate.

Pramanick discloses a polycrystalline gate that has a lower reaction barrier (see column 4, lines 45-50). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the gate electrode of the device of the Sakai reference in view of the Japanese patent as a polycrystalline gate to adjust the resistance value of the gate electrode.

9. Claims 22- 24, 47- 49, 59, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai in view of the Hattori and further in view of the Japanese patent.

With regards to claims 22, 23, 47, 48, 59, and 60, Sakai in view of the Hattori and the Japanese patent discloses the limitations in the claims, as discussed above. Note that the first gate electrode portion 4, which is opposite conductivity type as the body region of the Sakai device, would overly the first and second gate dielectric portions of the Hattori reference, if incorporated therein, and in the Sakai device.

With regard to claims 24 and 49, note that a third gate dielectric portion of the Hattori reference (at the right-hand-side of region 10), is approximately the same thickness as the first gate dielectric portion, and overlies the third gate dielectric portion.

10. Claims 25 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai in view of the Hattori and further in view of the Japanese patent as applied to claim 22 above, and further in view of Iwamuro.

Sakai in view of the Hattori and the Japanese patent discloses the limitations in the claims, as discussed above, but does not disclose the gate electrode portions are shorted together.

Iwamuro discloses in figure 1, gate portions 12 are shorted together, as can be seen in the figure. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the two gate portions function as one gate portion, while maintaining the advantages of having isolated gate portions.

11. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai in view of the Hattori and further in view of the Japanese patent as applied to claim 22 above, and further in view of Pramanick.

Sakai in view of the Japanese patent discloses the limitations in the claims, as discussed above, but does not disclose a polycrystalline gate.

Pramanick discloses a polycrystalline gate that has a lower reaction barrier (see column 4, lines 45-50). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the gate electrode of the device of the Sakai reference in view of the Japanese patent as a polycrystalline gate to adjust the resistance value of the gate electrode.

12. Claims 28, 31, 38, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai as applied to claim 1 above, and Sakai in view of Hattori (in

case of claim 38), and further in view of US Paten Application Publication 2003/0178689 (US SN 10/036,210) issued to Maszara et al., hereinafter Maszara, previously cited.

With regard to claim 28, Sakai discloses the limitations in the claims, as discussed above, except for different work functions of gate electrode portions.

Maszara discloses on page 2, paragraph 22, that different portions of a gate electrode region have different work functions. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the gate of the Sakai's device as having different work functions in order to have greater control over the inversion regions.

With regard to claims 31, 38 and 41, Sakai discloses the limitations in the claim, as discussed above, except for the body contact region being doped.

Maszara discloses doped gate electrode regions, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the body contact region 18 of the Sakai reference as a doped semiconductor region, since semiconductor electrodes are used extensively in the art and their resistances are more easily adjustable.

13. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai as applied to claim 1 above, and further in view of watanabe (US Patent 4,003,009), previously cited.

Sakai discloses the limitations in the claims, as discussed above, except for the circuitry comprising an inductor.

Watanabe discloses in figure 1, an inductor in combination with a capacitor, forming a resonant circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in the circuitry of Sakai an inductor in order to make a resonant circuitry.

14. Claim 75-78 and 83-86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai as applied to claims 1 and 39 above, and further in view of Benaissa et al. (US Patent Application Publication 2002/0074589), hereinafter the '589 reference, newly cited.

Regarding claims 75, 76, 78, 83, 84 and 86, Sakai substantially discloses the limitations in the claims, as discussed above, except for a field insulating region extending into the semiconductor body along a primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions; and a further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

The '589 reference discloses in figure 4, a varactor with isolation structures 30 surrounding a semiconductor island laterally (the semiconductor region between the two of the isolation structures). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include isolation trenches around the body region of the Sakai's varactor structure in order to insulate the regions of the device from the neighboring regions of the semiconductor devices which are present on a

substrate, when the varactor structure is used in a circuitry along with the other semiconductor devices.

Regarding claim 77 and 85, a further semiconductor island (the one between the two most right insulating regions 30) would have been occupied by material of the body if it were to be used in the varactor structure of Sakai.

15. Claims 79-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai in view of Hattori as applied to claim 34 above, and further in view of the '589 reference.

Sakai in view of Hattori renders obvious the claimed invention, as discussed above, except for a field insulating region extending into the semiconductor body along a primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions; and a further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

The '589 reference discloses these limitations, as discussed above with respect to claims 75-78, and as to why one of ordinary skill in the art would want to use the trench insulators. Therefore, that part of the rejection will not be repeated here.

16. Claims 87-94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai and the Japanese patent as applied to claim 42 above, and further in view of the '589 reference.

Sakai in view of the Japanese patent renders obvious the claimed invention, as discussed above, except for a field insulating region extending into the semiconductor body along a primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions; and a further semiconductor island occupied by material of the body region substantially up to the primary surface such that material of the body region extends continuously from each semiconductor island to each other semiconductor island.

The '589 reference discloses these limitations, as discussed above with respect to claims 75-78, and as to why one of ordinary skill in the art would want to use the trench insulators. Therefore, that part of the rejection will not be repeated here.

Response to Arguments

17. Applicant's arguments filed on 11/23/04 with respect to the newly added claims 75-94 have been considered and are believe as being addressed in the above rejections with respect to those claims.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER